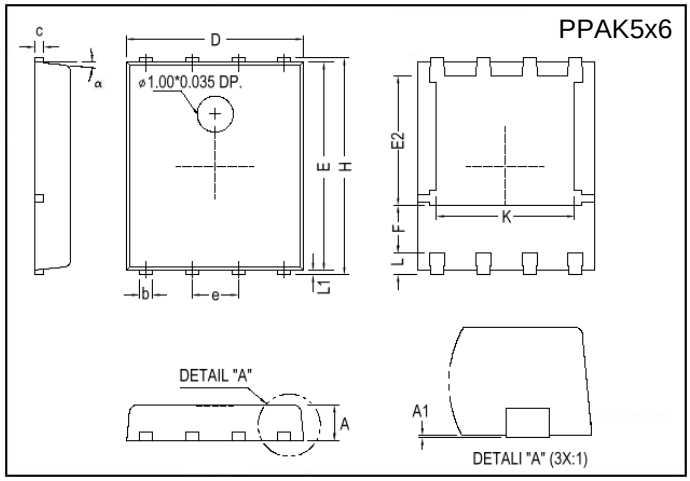
YEA SHIN TECHNOLOGY CO., LTD

YS60P03BA

P-Channel Enhancement MOSFET

VDS= -30V, ID= -60A

PPAK5x6



DESCRIPTION

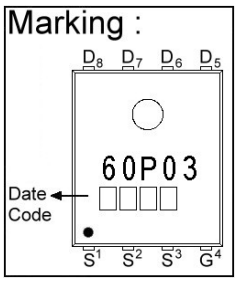
The YS60P03BA is using trench DMOS technology. This advanced technology has been especially tailored to minimize $R_{DS(ON)}$ provide superior switching performance, and withstand high energy pulse in the avalanche and commutation made. These devices are well suited for high efficiency fast switching applications.

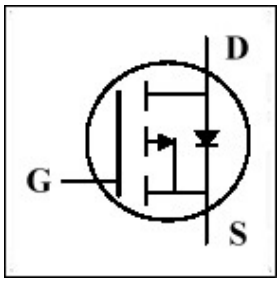
The YS60P03BA meet the RoHS and Green Product requirement, 100% EAS and Rg guaranteed with full function reliability approved.

FEATURES

- Advanced DMOS Trench technology
- Suit for -4.5V Gate Drive Application
- Green Device Available
- Fast switching
- 100% EAS and Rg Guaranteed

REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.85	1.00	1.15	E	5.70	-	5.90
A1	0.00	-	0.10	e	-	1.27	-
b	0.30	-	0.51	H	5.90	-	6.20
c	0.20	-	0.30	L	-	0.60	-
D	4.80	-	5.00	L1	0.06	-	0.20
F	1.10REF.			α	0°	-	12°
E2	3.50REF.			K	3.70	3.90	4.10





Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current [1]	I_D @T_C=25℃	-60	A
	I_D @T_C=100℃	-38	A
Pulsed Drain Current[1,2]	I_{DM}	-240	A
Total Power Dissipation[4]	P_D @T_C=25℃	96	W
	P_D @T_A=25℃	2	W
Single Pulse Avalanche Energy, L=0.1mH[3]	E_{AS}	168	mJ
Single Pulse Avalanche Current, L=0.1mH[3]	I_{AS}	-58	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient[1]	$R_{\theta JA}$	Steady State	62.5	℃/W
Thermal Resistance Junction-case[1]	$R_{\theta JC}$	Steady State	1.3	℃/W

DEVICE CHARACTERISTICS

YS60P03BA

Electrical Characteristics (Tj = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	V_{GS}=0, I_D=-250uA
Gate Threshold Voltage	$V_{GS(th)}$	-1.2	-1.6	-2.5	V	V_{DS}=V_{GS}, I_D=-250uA
Forward Transconductance	g_{fs}	-	14	-	S	V_{DS}=-10V, I_D=-10A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current(Tj=25℃)	I_{DSS}	-	-	-1	uA	V_{DS}=-30V, V_{GS}=0
Drain-Source Leakage Current(Tj=125℃)		-	-	-10	uA	V_{DS}=-24V, V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	7.2	8.5	mΩ	V_{GS}=-10V, I_D=-20A
		-	11.5	14		V_{GS}=-4.5V, I_D=-16A
Total Gate Charge[2]	Q_g	-	35	-	nC	I_D=-10A V_{DS}=-15V V_{GS}=-4.5V
Gate-Source Charge	Q_{gs}	-	10.8	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	10.6	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	24.5	-	ns	V_{DD}=-15V I_D=-1A V_{GS}=-10V R_G=6Ω
Rise Time	T_r	-	10.5	-		
Turn-off Delay Time	$T_{d(off)}$	-	157	-		
Fall Time	T_f	-	50	-		
Input Capacitance	C_{iss}	-	3300	-	pF	V_{GS}=0V V_{DS}=-15V f=1.0MHz
Output Capacitance	C_{oss}	-	410	-		
Reverse Transfer Capacitance	C_{rss}	-	280	-		

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy[5]	EAS	20	-	-	mJ	V_{DD}=-25V, L=0.1mH, I_{AS}=-20A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage[2]	V_{SD}	-	-	-1.2	V	V_{GS}=0V, I_S=-20A , T_J=25℃
Continuous Source Current[1,6]	I_S	-	-	-60	A	V_G=V_D=0V, Force Current
Pulsed Source Current[2,6]	I_{SM}	-	-	-120	A	

Notes: **1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.**

2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3. The EAS data shows Max. rating. The test condition is VDD=-25V, VGS=-10V, L=0.1mH, IAS=-58A.

4. The power dissipation is limited by 150℃ junction temperature.

5. The Min. value is 100% EAS tested guarantee.

6. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

DEVICE CHARACTERISTICS

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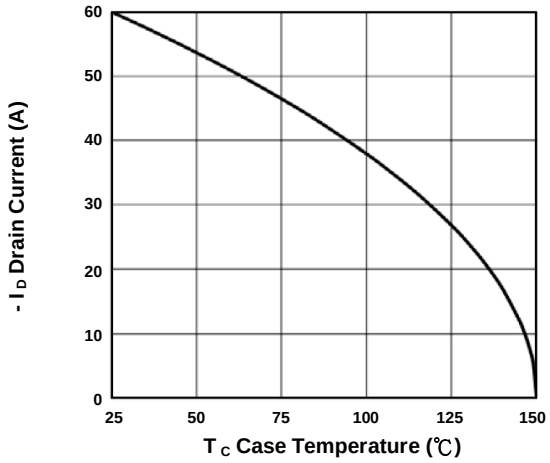

Fig.1 Drain Current vs. T_C

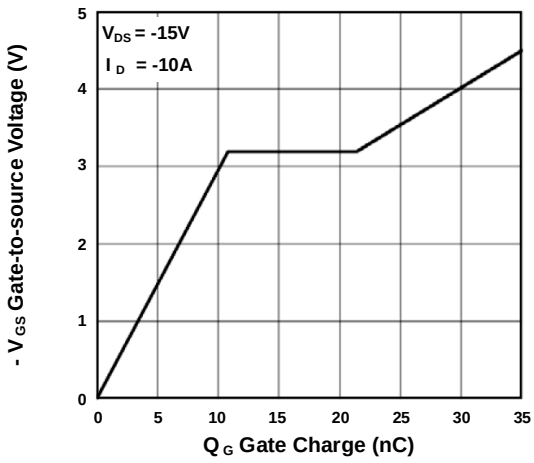

Fig.2 Gate Charge Characteristics

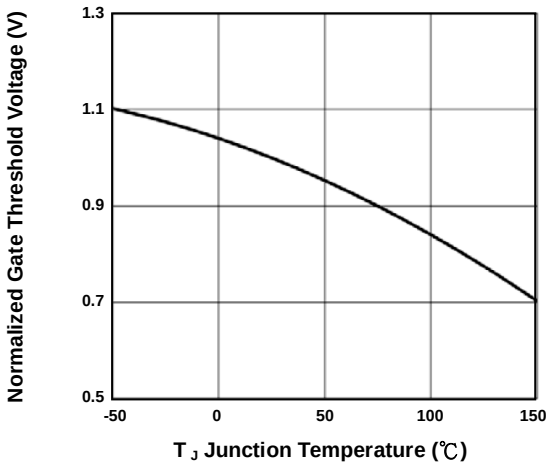

Fig.3 Normalized $V_{GS(th)}$ vs. T_J

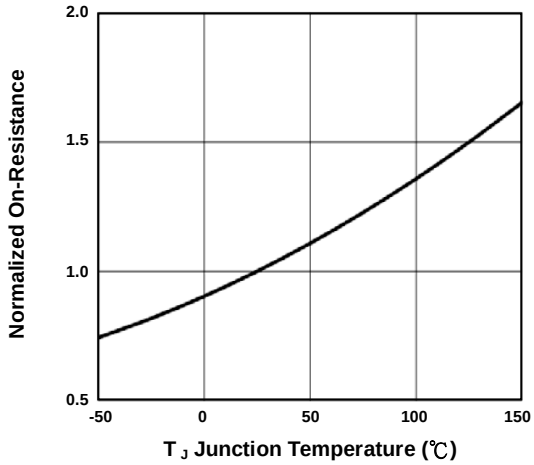

Fig.4 Normalized R_{DSON} vs. T_J

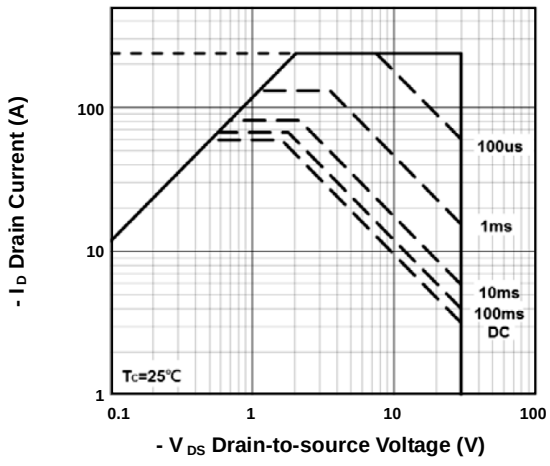

Fig.5 Safe Operating Area

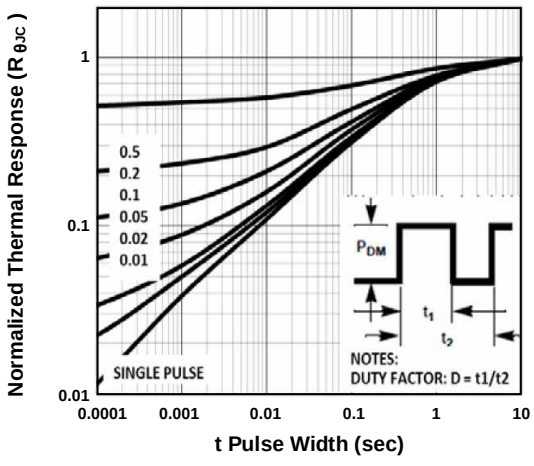

Fig.6 Transient Thermal Impedance

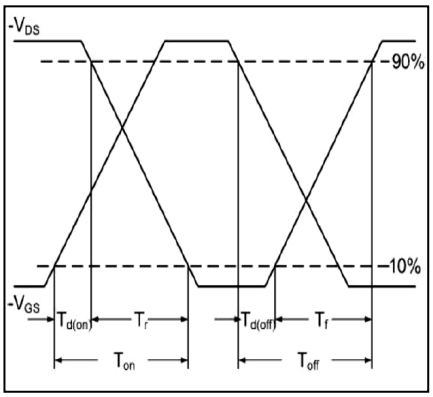

Fig.7 Switching Time Waveform

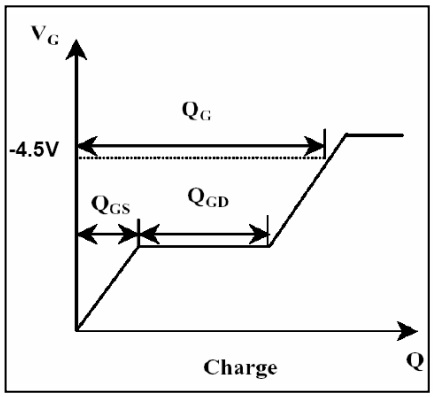

Fig.8 Gate Charge Waveform