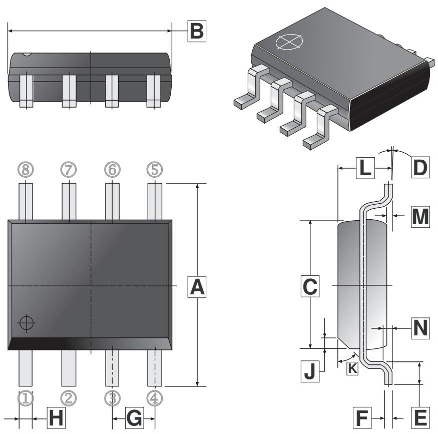
**YEA SHIN TECHNOLOGY CO., LTD**

# YS4953M

# Dual P-Channel Enhancement MOSFET

## VDS= -30V, ID= -6A

SOP-8




## DESCRIPTION

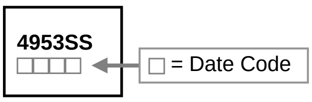
The YS4953M uses advanced trench technology to provide excellent on-resistance, low gate charge and operation with gate voltages as low as 2.5V. The device is suitable for use as a load switch or in PWM applications. It may be used in a common drain arrangement to from a bidirectional blocking switch.

## FEATURES

- Simple Drive Requirement
- Lower On-resistance
- Low Gate Charge

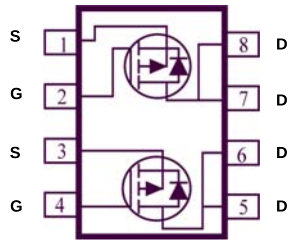
| REF. | Millimeter Min. | Millimeter Max. | REF. | Millimeter Min. | Millimeter Max. |
|---|---|---|---|---|---|
| A | 5.79 | 6.20 | H | 0.33 | 0.51 |
| B | 4.70 | 5.11 | J | 0.375 REF. | |
| C | 3.70 | 4.10 | K | 45°REF. | |
| D | 0° | 8° | L | 1.30 | 1.752 |
| E | 0.38 | 1.27 | M | 0.10 | 0.25 |
| F | 0.10 | 0.26 | N | 0.25 REF. | |
| G | 1.27 TYP. | | | | |

## MARKING




## PACKAGE INFORMATION

| Package | MPQ | Leader Size |
|---|---|---|
| SOP-8 | 3K | 13' inch |




## MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise specified)

| Parameter | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current @ $V_{GS}$=10V [1] | $T_A$ = 25°C | $I_D$ | -6 | A |
| | $T_A$ = 100°C | | -4 | |
| Pulsed Drain Current [2] | | $I_{DM}$ | -12 | A |
| Single Pulse Avalanche Energy [3] | | EAS | 108 | mJ |
| Avalanche Current | | $I_{AS}$ | 19 | A |
| Total Power Dissipation [4] | $T_A$ = 25°C | $P_D$ | 1.5 | W |
| Operating Junction & Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 ~ 150 | °C |
| **Thermal Resistance Ratings** | | | | |
| Thermal Resistance Junction-Ambient [1] (Max.) | | $R_{\theta JA}$ | 83 | °C / W |
| Thermal Resistance Junction-Case [1] (Max.) | | $R_{\theta JC}$ | 60 | °C / W |

## ELECTRICAL CHARACTERISTICS ($T_j$ = 25°C unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test condition |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | -30 | - | - | V | $V_{GS}$=0V, $I_D$= -250μA |
| Gate-Threshold Voltage | $V_{GS(th)}$ | -1 | - | -2.5 | V | $V_{DS}$=$V_{GS}$, $I_D$ = -250μA |
| Forward Transfer Conductance | $G_{fs}$ | - | 6 | - | S | $V_{DS}$= -10V, $I_D$= -6A |
| Gate-Body Leakage | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$=±20V |
| Drain-Source Leakage Current | $I_{DSS}$ | - | - | -1 | μA | $V_{DS}$= -24V,$V_{GS}$=0 |
| Drain-Source On-Resistance [2] | $R_{DS(ON)}$ | - | - | 45 | mΩ | $V_{GS}$= -10V, $I_D$ = -5A |
| | | - | - | 82 | | $V_{GS}$= -4.5V, $I_D$ = -4A |
| Total Gate Charge | $Q_g$ | - | 6.4 | - | nC | $I_D$= -6A<br>$V_{DS}$= -20V<br>$V_{GS}$= -4.5V |
| Gate-Source Charge | $Q_{gs}$ | - | 2.7 | - | | |
| Gate-Drain ("Miller") Charge | $Q_{gd}$ | - | 3.1 | - | | |
| Turn-On Delay Time [2] | $T_{d(on)}$ | - | 9 | - | nS | $V_{DS}$= -12V<br>$I_D$= -5A<br>$V_{GS}$= -10V<br>$R_G$= 3.3Ω |
| Rise Time | $T_r$ | - | 16.6 | - | | |
| Turn-Off Delay Time | $T_{d(off)}$ | - | 21 | - | | |
| Fall Time | $T_f$ | - | 21.6 | - | | |
| Input Capacitance | $C_{iss}$ | - | 645 | - | pF | $V_{GS}$=0V<br>$V_{DS}$= -25V<br>f=1.0MHz |
| Output Capacitance | $C_{oss}$ | - | 272 | - | | |
| Reverse Transfer Capacitance | $C_{rss}$ | - | 105 | - | | |
| **Avalanche Characteristics** | | | | | | |
| Single Pulse Avalanche Energy [5] | EAS | 30 | - | - | mJ | $V_{DD}$= -25V, L=0.1mH, $I_{AS}$= -10A |
| **Source-Drain Diode** | | | | | | |
| Forward On Voltage [2] | $V_{DS}$ | - | -0.84 | -1.2 | V | $I_S$= -1.7A, $V_{GS}$=0V |
| Continuous Source Current [1,6] | $I_S$ | - | - | -6 | nS | $V_G$= $V_D$=0V<br>Force Current |
| Pulsed Source Current [2,6] | $I_{SM}$ | - | - | -12 | nC | |

Notes:

1. surface mounted on a 1 inch2 FR-4 board with 2OZ copper. 135℃/W when mounted on Min. copper pad.
2. The data tested by pulsed , pulse width≦300us , duty cycle≦2%
3. The EAS data shows Max. rating . The test condition is $V_{DD}$= -25V,$V_{GS}$= -10V,L=0.1mH,$I_{AS}$= -19A
4. The power dissipation is limited by 150℃ junction temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## CHARACTERISTIC CURVES

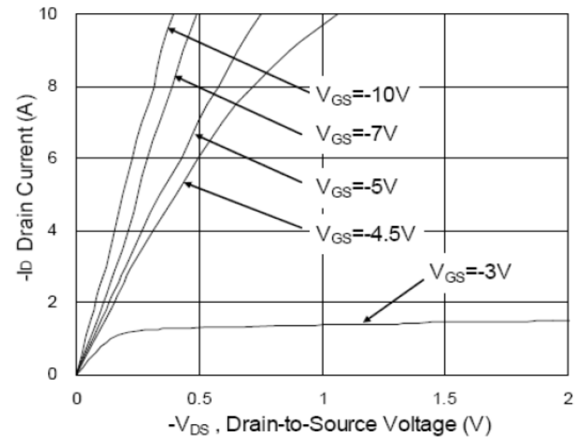



**Fig.1 Typical Output Characteristics**

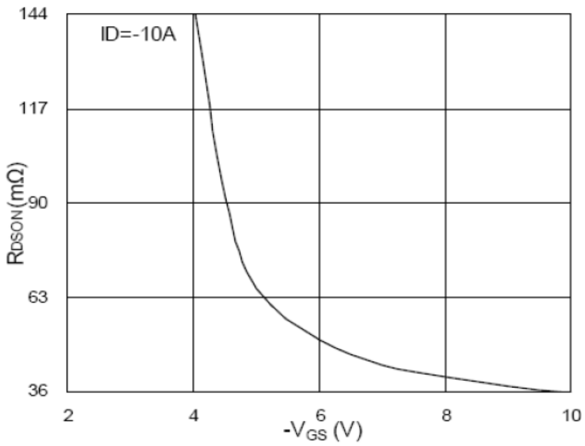



**Fig.2 On-Resistance vs. Gate-Source**

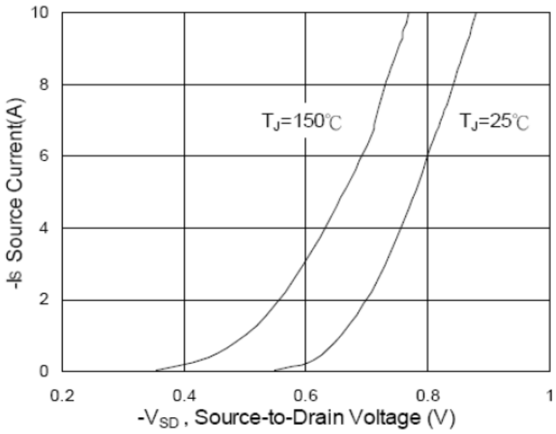



**Fig.3 Forward Characteristics of Reverse**

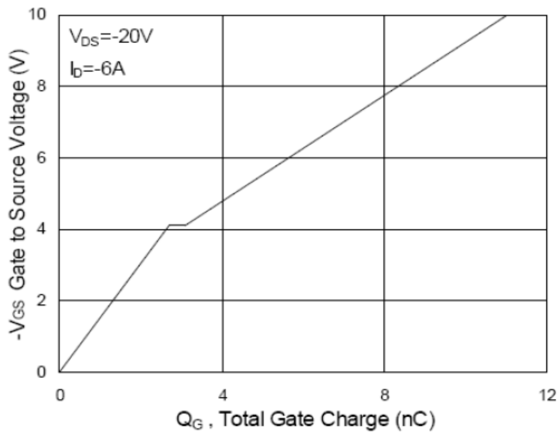



**Fig.4 Gate-charge Characteristics**

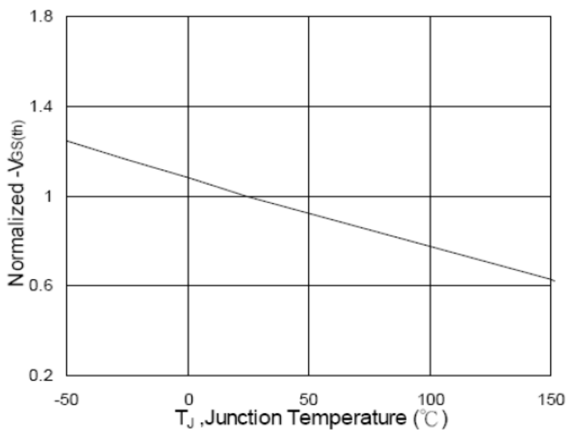



**Fig.5 Normalized $V_{GS(th)}$ vs. $T_J$**

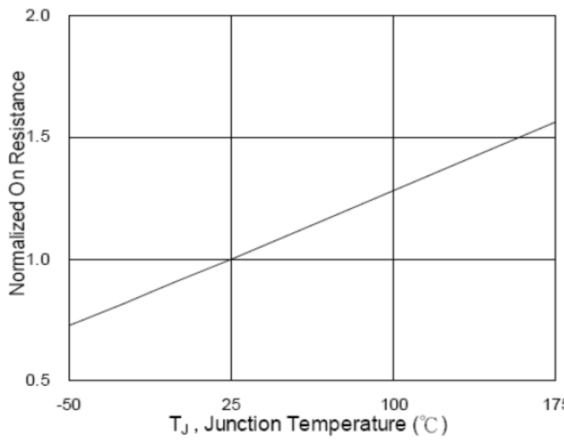



**Fig.6 Normalized $R_{DSON}$ vs. $T_J$**

## CHARACTERISTIC CURVES

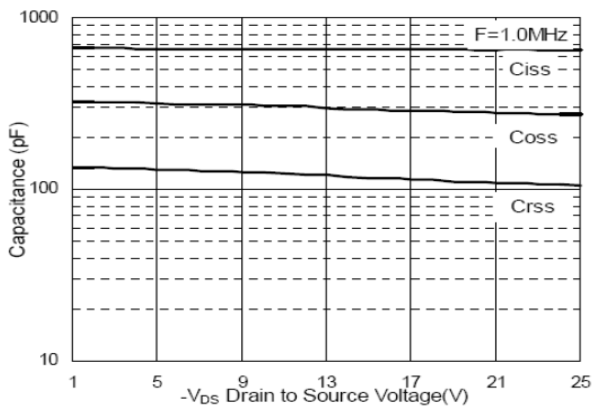



**Fig.7 Capacitance**

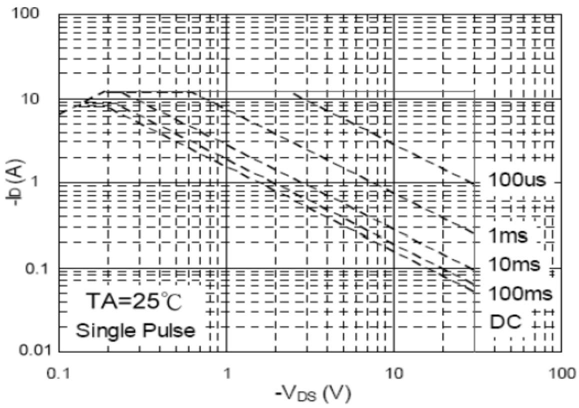



**Fig.8 Safe Operating Area**

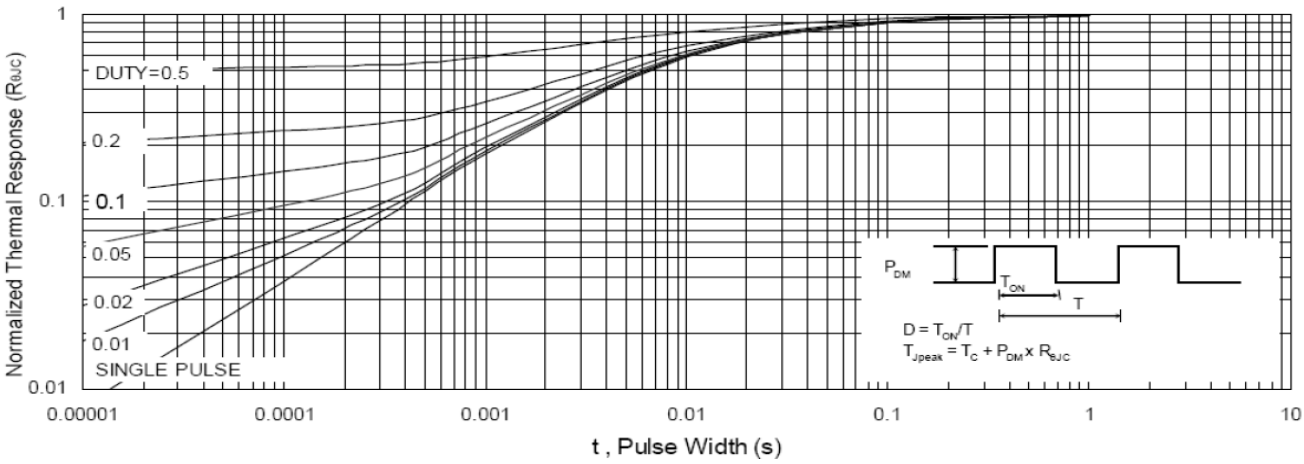



**Fig.9 Normalized Maximum Transient Thermal Impedance**

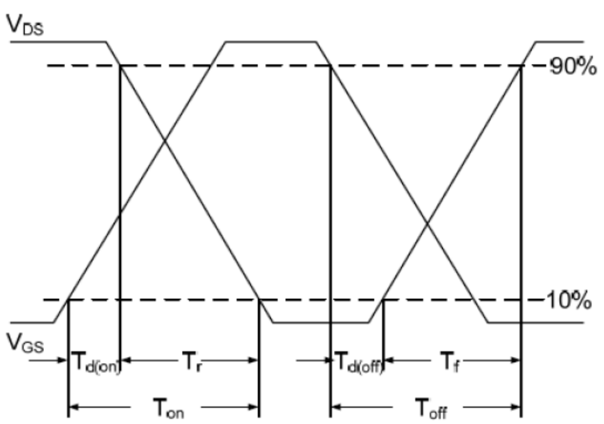



**Fig.10 Switching Time Waveform**

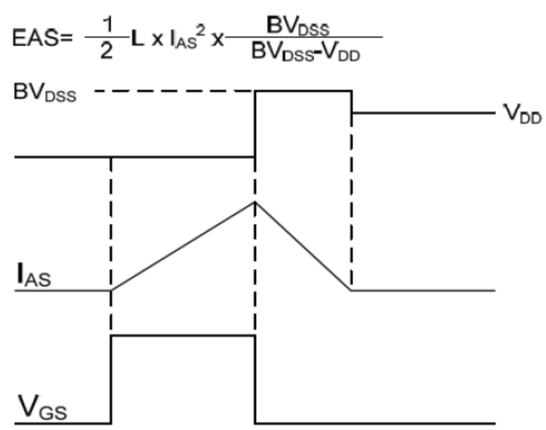



**Fig.11 Unclamped Inductive Switching Wave**