YEA SHIN TECHNOLOGY CO., LTD

YS30N06BB

N-Channel Enhancement MOSFET

VDS= 30V, ID= 40A[3]

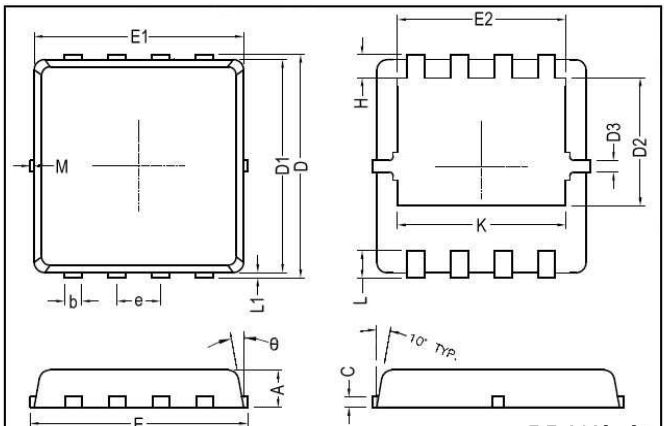
DESCRIPTION

The YS30N06BB uses advanced Trench technology and designs to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

The YS30N06BB meet the RoHS and Green Product requirement, 100% EAS and 100% Rg guaranteed with full function reliability approved.

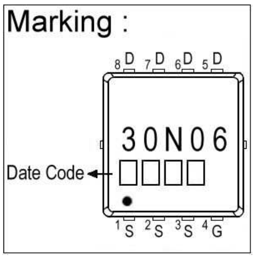
FEATURES

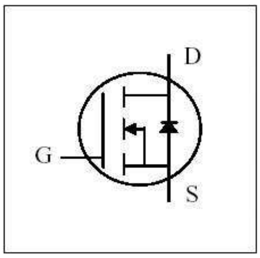
- Low On-Resistance
- Low Input Capacitance
- Green Device Available
- Low Miller Charge
- 100% EAS and 100% Rg Guaranteed



PPAK3x3

REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.70	0.75	0.80	E1	3.00	3.15	3.20
b	0.25	0.30	0.35	E2	2.39	2.49	2.59
C	0.10	0.15	0.25	e	0.65 BSC		
D	3.25	3.35	3.45	H	0.30	0.39	0.50
D1	3.00	3.10	3.20	L	0.30	0.40	0.50
D2	1.48	1.58	1.68	L1	-	0.13	0.20
D3	-	0.13	-	θ	-	10°	12°
E	3.20	3.30	3.40	M	-	-	0.15





Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D @T_A=25℃	25	A
	I_D @T_A=70℃	20	A
Pulsed Drain Current[1]	I_{DM}	100	A
Continuous Drain Current[3]	I_D @T_C=25℃	40	A
	I_D @T_C=70℃	40	A
Total Power Dissipation	P_D @T_C=25℃	52	W
	P_D @T_A=25℃	3.8	W
Single Pulse Avalanche Energy, L=0.1mH	E_{AS}	72	mJ
Single Pulse Avalanche Current, L=0.1mH	I_{AS}	38	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient[2]	$R_{\theta JA}$	t ≤ 10s	33	℃/W
Thermal Resistance Junction-case[2]	$R_{\theta JC}$	Steady State	2.4	℃/W

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Electrical Characteristics (Tj = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250uA
Gate Threshold Voltage	$V_{GS(th)}$	1.15	-	2.2	V	V_{DS}=V_{GS}, I_D=250uA
Forward Transconductance[1]	g_{fs}	-	82	-	S	V_{DS}=15V, I_D=19A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	V_{DS}=30V, V_{GS}=0
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	3.4	4.8	mΩ	V_{GS}=10V, I_D=19A
		-	4.7	5.8		V_{GS}=4.5V, I_D=16A
Total Gate Charge	Q_g	-	12	-	nC	I_D=19A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge	Q_{gs}	-	6	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	5	-		
Turn-on Delay Time	$T_{d(on)}$	-	24	-	ns	V_{DS}=15V I_D=10A V_{GS}=4.5V R_G=1Ω R_L=1.5Ω
Rise Time	T_r	-	21	-		
Turn-off Delay Time	$T_{d(off)}$	-	25	-		
Fall Time	T_f	-	17	-		
Input Capacitance	C_{iss}	-	1750	-	pF	V_{GS}=0V V_{DS}=15V f=1.0MHz
Output Capacitance	C_{oss}	-	360	-		
Reverse Transfer Capacitance	C_{rss}	-	150	-		
Gate Resistance	R_g	-	3.2	-	Ω	f=1.0MHz

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy[4]	EAS	48	-	-	mJ	V_{DD}=20V, L=0.1mH, I_{AS}=31A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Max. Body-Diode Continuous Current	I_S	-	-	40	A	-
Diode Forward Voltage	V_{SD}	-	0.8	1.2	V	I_S=10A, V_{GS}=0V
Reverse Recovery Time	t_{rr}	-	25	-	ns	I_F=10A, dI/dt=100A/μs, T_J=25℃
Reverse Recovery Charge	Q_{rr}	-	17	-	nC	

Notes: **1. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.**

2. $R_{θJA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{θJC}$ is guaranteed by design while $R_{θCA}$ is determined by the user's board design. $R_{θJA}$ shown below for single device operation on FR-4 in still air.

3. The maximum current rating is limited by package.

4. The Min. value is 100% EAS tested guarantee.

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Typical Characteristics

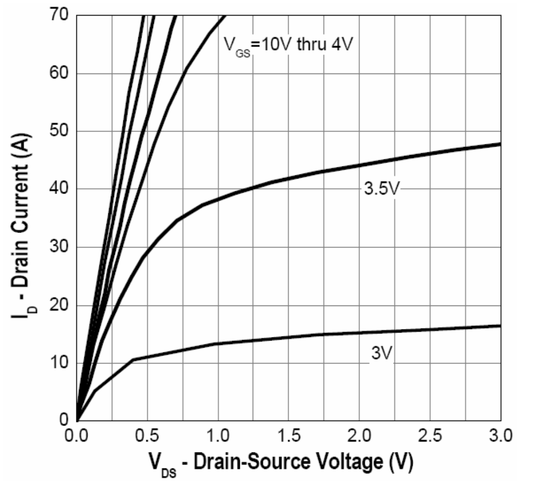

Fig.1 Typical Output Characteristics

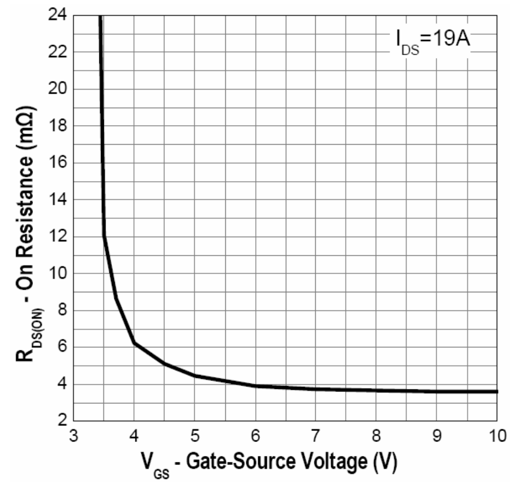

Fig.2 On-Resistance vs. G-S Voltage

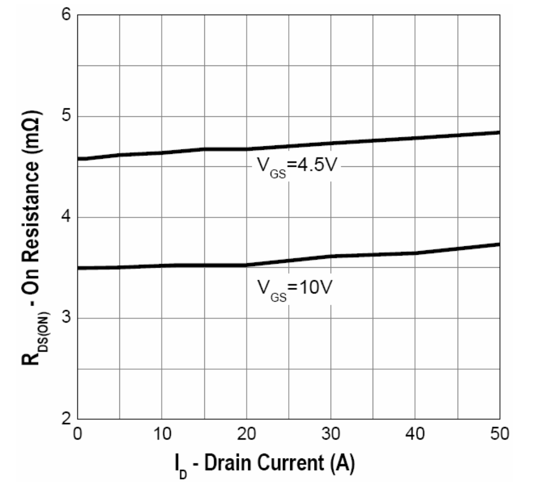

Fig.3 On-Resistance vs. Drain Current

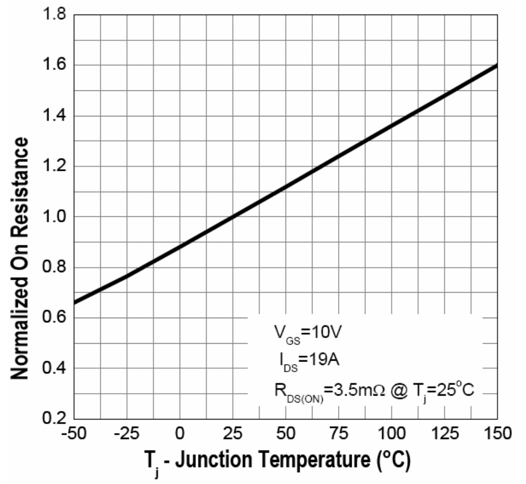

Fig.4 Normalized R_{DSON} vs. T_J

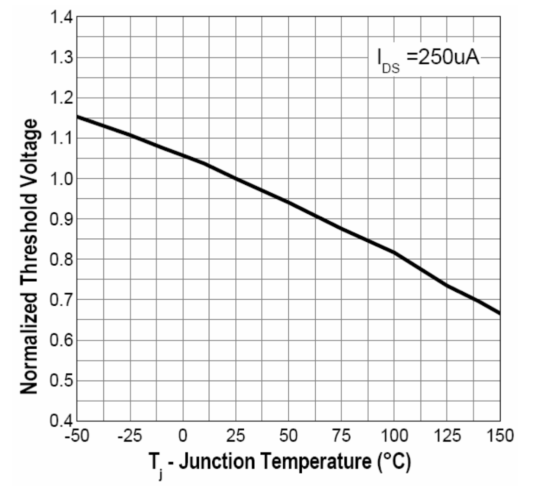

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

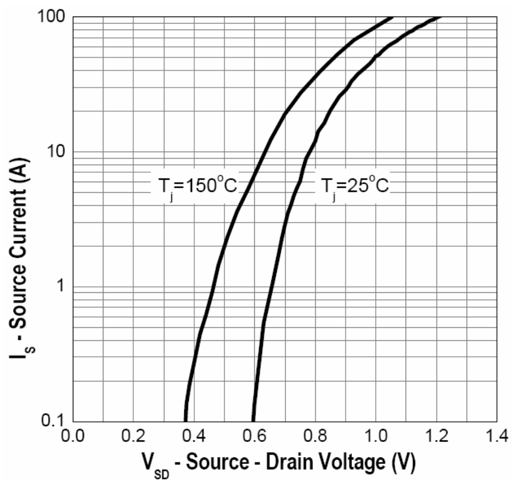

Fig.6 Forward Characteristics of Reverse

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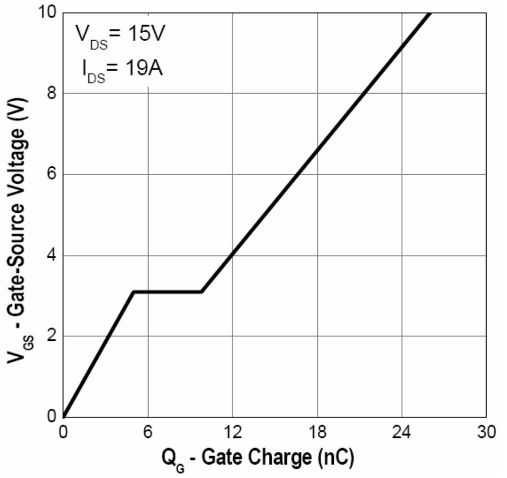

Fig.7 Gate Charge Characteristics

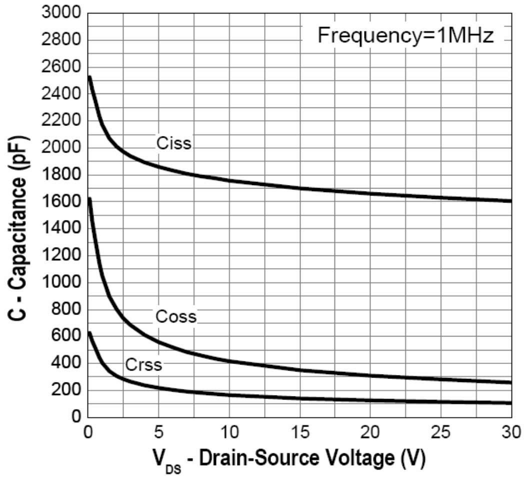

Fig.8 Capacitance Characteristics

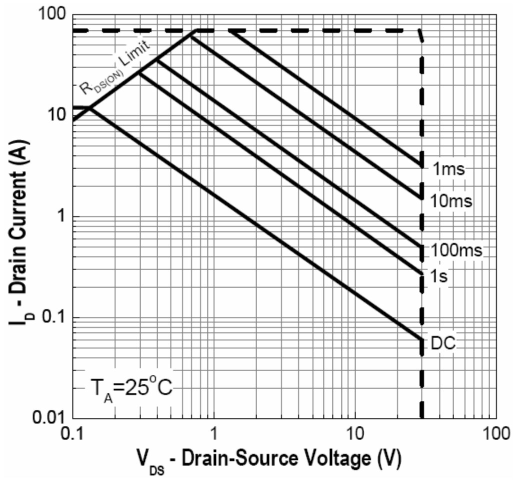

Fig.9 Safe Operating Area

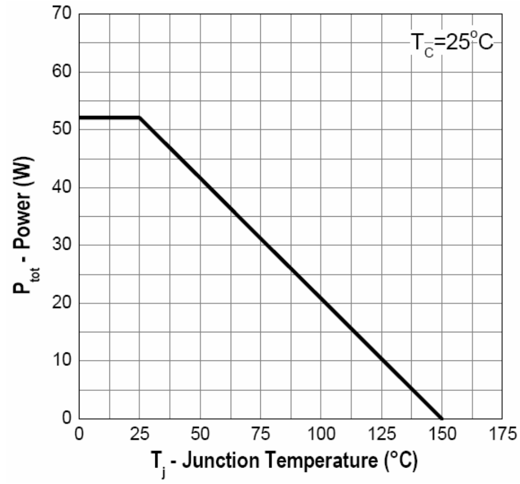

Fig.10 Power Dissipation

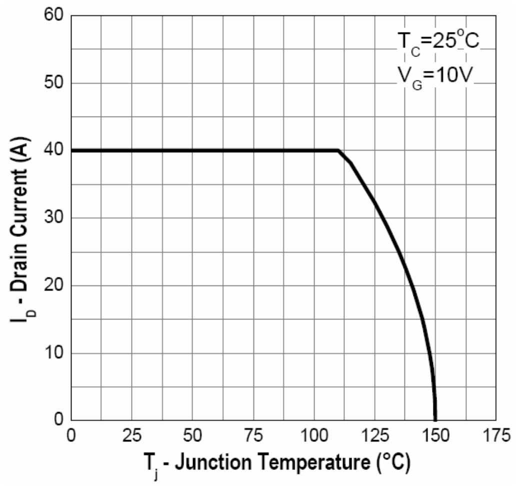

Fig.11 Drain Current vs. T_J

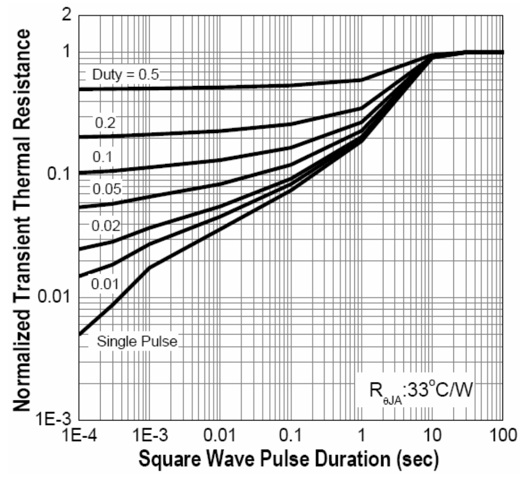

Fig.12 Transient Thermal Impedance