N-Channel Enhancement MOSFET

VDS = 100V, ID = 42A

DESCRIPTION

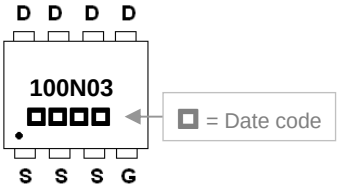
The YS100N03BA uses avanced Trench technology designs to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM load switching and general purpose applications.

TheYS100N03BA meet the RoHS and Green Product requirement,100% EAS guaranteed with full function reliability approved.

FEATURES

- Low On-Resistance
- Low Input Capacitance
- Green Device Available
- Low Miller Charge
- 100% EAS Guaranteed

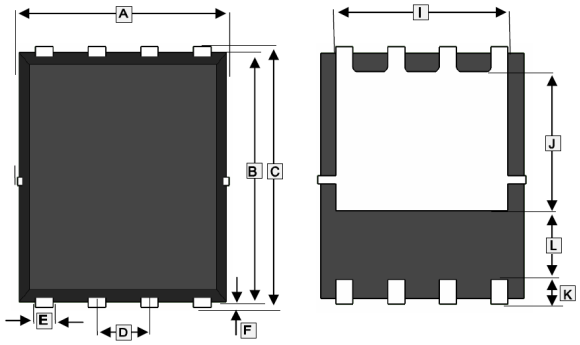
MARKING



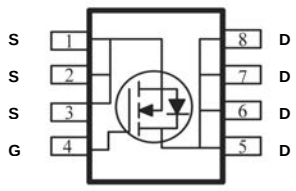
PACKAGE INFORMATION

Package	MPQ	Leader Size
PPAK5x6	3K	13 inch

PPAK5x6



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.8	5.1	G	0.8	1.1
B	5.7	5.9	H	0.254 Ref.	
C	5.9	6.2	I	4.0 Ref.	
D	1.27 BSC.		J	3.4 Ref.	
E	0.33	0.51	K	0.6 Ref.	
F	0.1	0.2	L	1.4 Ref.	



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current[1]	I_D @T_C=25℃	42	A
	I_D @T_C=70℃	34	A
Pulsed Drain Current[1]	I_{DM}	150	A
Continuous Drain Current	I_D @T_A=25℃	6.6	A
	I_D @T_A=70℃	5.3	A
Total Power Dissipation	P_D @T_C=25℃	83.3	W
	P_D @T_A=25℃	3.6	W
Single Pulse Avalanche Energy, L=3mH	E_{AS}	63	mJ
Single Pulse Avalanche Current, L=3mH	I_{AS}	6.5	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient[2]	$R_{\theta JA}$	Steady State	35	℃/W
Thermal Resistance Junction-case[2]	$R_{\theta JC}$	Steady State	1.5	℃/W

DEVICE CHARACTERISTICS

YS100N03BA

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	V_{GS}=0, I_D=250uA
Gate Threshold Voltage	$V_{GS(th)}$	1.2	1.8	2.5	V	V_{DS}=V_{GS}, I_D=250uA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	V_{DS}=80V, V_{GS}=0
Static Drain-Source On-Resistance[1]	$R_{DS(ON)}$	-	20	25	mΩ	V_{GS}=10V, I_D=10A
		-	22	28.5		V_{GS}=4.5V, I_D=10A
Total Gate Charge[1]	Q_g	-	34	-	nC	I_D=10A V_{DS}=50V V_{GS}=10V
Gate-Source Charge	Q_{gs}	-	6	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	9	-		
Turn-on Delay Time[1]	$T_{d(on)}$	-	7	-	ns	V_{DS}=50V V_{GS}=10V R_G=3Ω R_L=5Ω
Rise Time	T_r	-	7	-		
Turn-off Delay Time	$T_{d(off)}$	-	29	-		
Fall Time	T_f	-	7	-		
Input Capacitance	C_{iss}	-	1325	-	pF	V_{GS}=0V V_{DS}=30V f=1.0MHz
Output Capacitance	C_{oss}	-	110	-		
Reverse Transfer Capacitance	C_{rss}	-	64	-		

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy[3]	EAS	34.5	-	-	mJ	V_{DD}=50V, L=3mH, I_{AS}=4.8A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage	V_{SD}	-	-	1.3	V	I_S=10A, V_{GS}=0V
Reverse Recovery Time	t_{rr}	-	32	-	ns	I_F=10A, dI/dt=500A/μs, T_J=25℃
Reverse Recovery Charge	Q_{rr}	-	200	-	nC	

Notes: **1. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.**

2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.

3. The Min. value is 100% EAS tested guarantee.

DEVICE CHARACTERISTICS

YS100N03BA

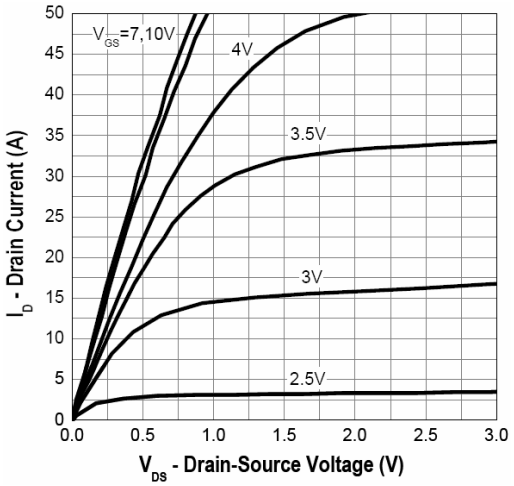


Fig.1 Typical Output Characteristics

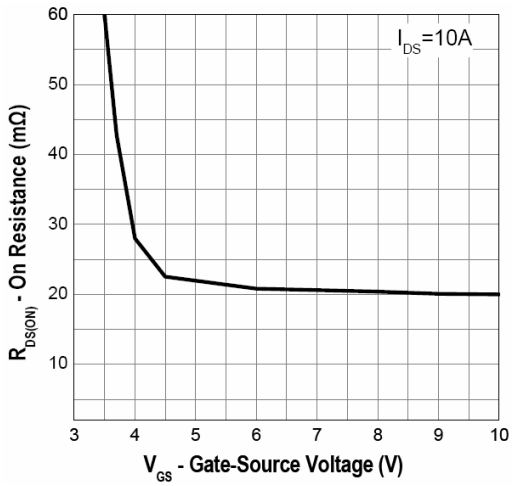


Fig.2 On-Resistance vs. G-S Voltage

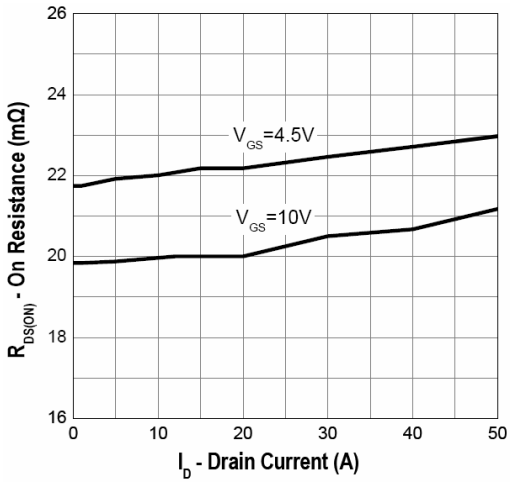


Fig.3 On-Resistance vs. Drain Current

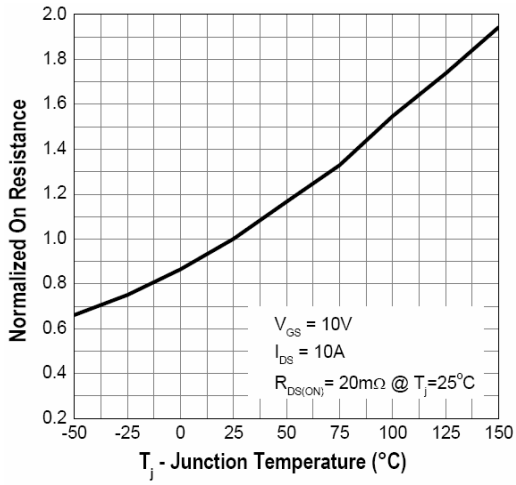


Fig.4 Normalized R_{DSON} vs. T_J

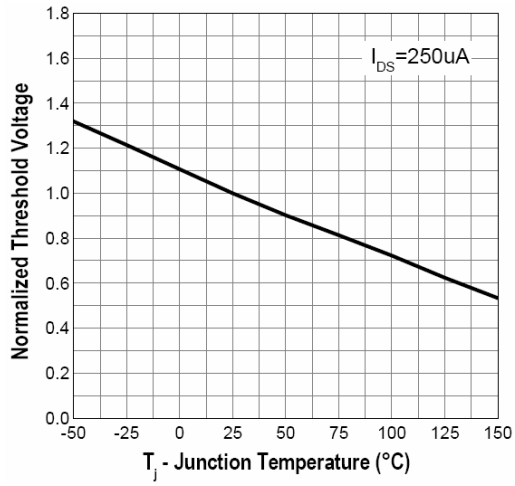


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

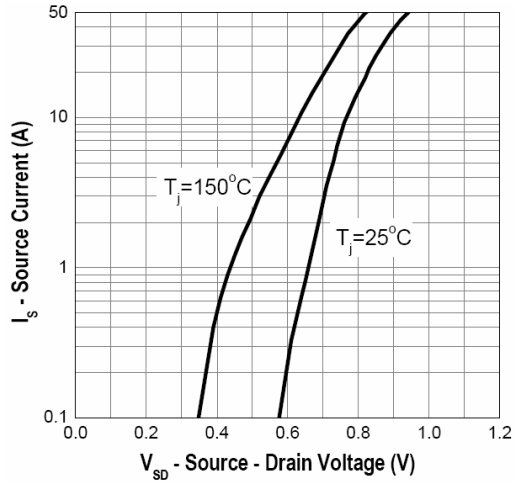


Fig.6 Forward Characteristics of Reverse

DEVICE CHARACTERISTICS

YS100N03BA

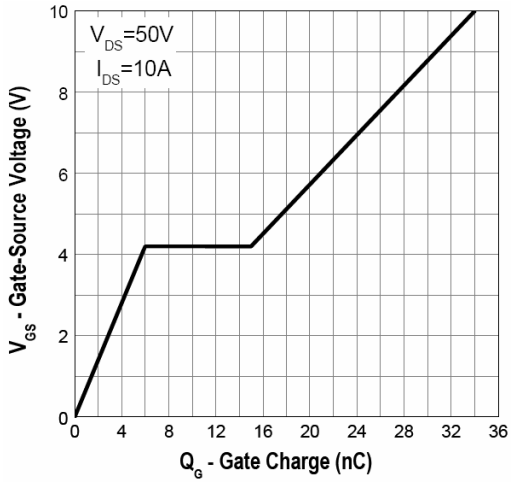


Fig.7 Gate Charge Characteristics

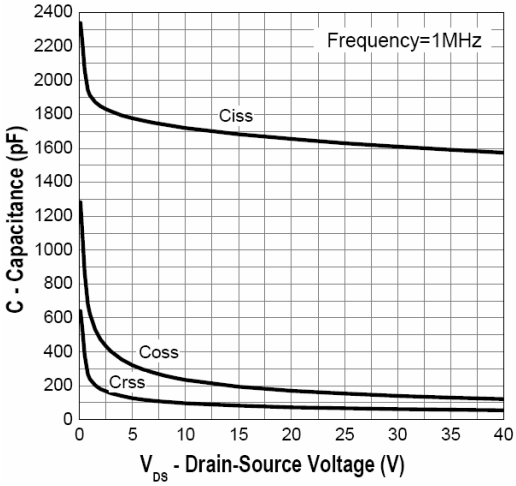


Fig.8 Capacitance Characteristics

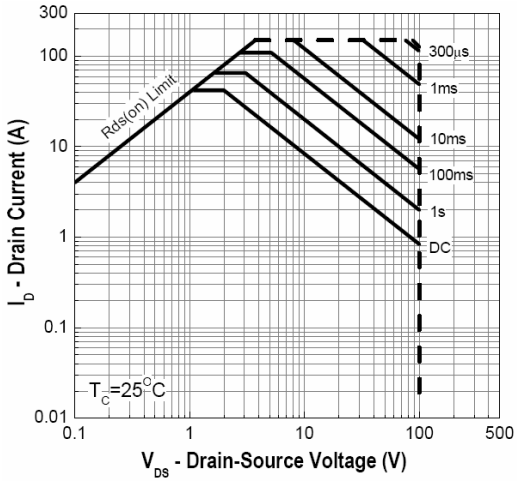


Fig.9 Safe Operating Area

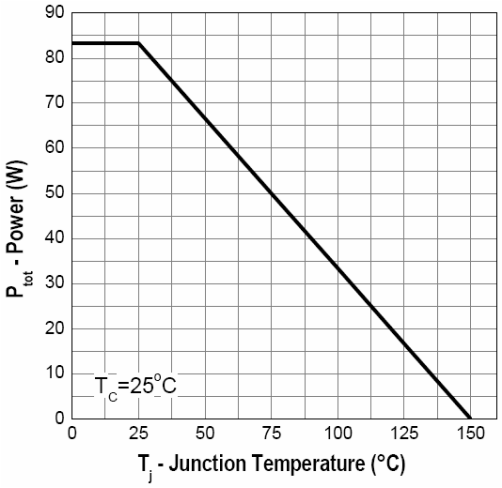


Fig.10 Power Dissipation

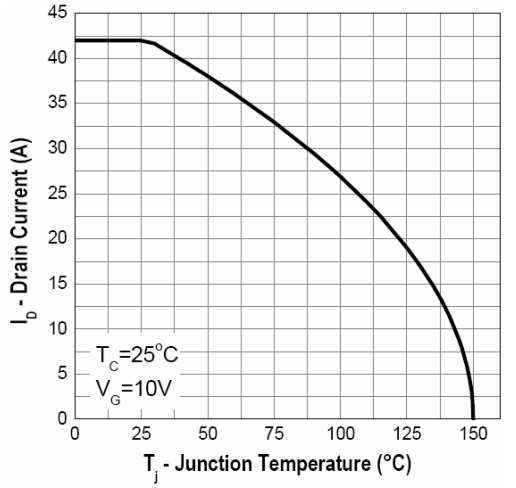


Fig.11 Drain Current vs. T_J

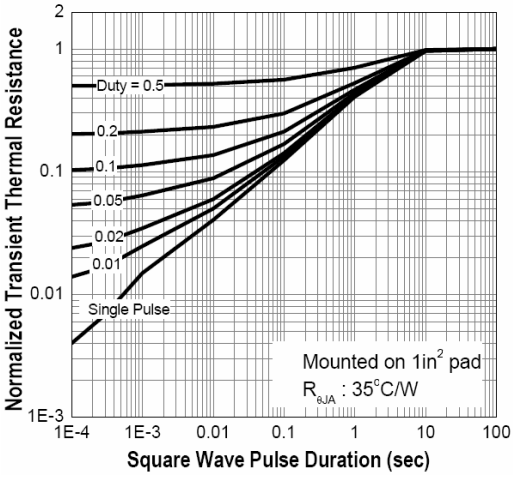


Fig.12 Transient Thermal Impedance