



YEA SHIN TECHNOLOGY CO., LTD

YS09N10D

N-Channel Enhancement MOSFET
VDS= 100V, ID= 9A

Pb H

DESCRIPTION

The YS09N10D is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications .

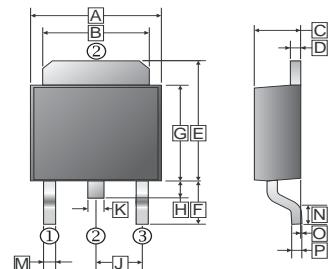
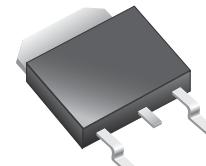
FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

MARKING



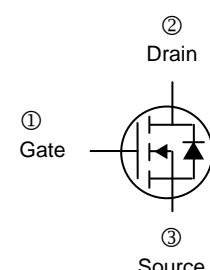
TO-252(D-Pack)



PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30	REF
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}=10\text{V}^1$	I_D	9	A
		5.7	A
Pulsed Drain Current ²	I_{DM}	18	A
Total Power Dissipation ³	P_D	31	W
		2	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	°C
Thermal Resistance Rating			
Maximum Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	4	°C / W
Maximum Thermal Resistance Junction-ambient ¹	$R_{\theta JA}$	62	°C / W

YS09N10D

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	$\text{V}_{\text{GS}}=0, \text{I}_D=250\mu\text{A}$
Breakdown Voltage Temperature Coefficient	$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	-	0.122	-	V/ $^\circ\text{C}$	Reference to 25°C , $\text{I}_D=1\text{mA}$
Gate-Threshold Voltage	$\text{V}_{\text{GS}(\text{th})}$	1	-	2.5	V	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$\text{V}_{\text{GS}}= \pm 20\text{V}$
Forward Transconductance	g_{fs}	-	19	-	S	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=8\text{A}$
Drain-Source Leakage Current	$T_J=25^\circ\text{C}$	I_{DSS}	-	-	1	μA
	$T_J=55^\circ\text{C}$		-	-	30	
Static Drain-Source On-Resistance ²	$\text{R}_{\text{DS}(\text{ON})}$	-	-	152	$\text{m}\Omega$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=8\text{A}$
		-	-	158		$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_D=6\text{A}$
Total Gate Charge ²	Q_g	-	25.5	-	nC	$\text{I}_D=8\text{A}$ $\text{V}_{\text{DS}}=60\text{V}$ $\text{V}_{\text{GS}}=10\text{V}$
Gate-Source Charge	Q_{gs}	-	4.2	-		
Gate-Drain ("Miller") Change	Q_{gd}	-	4.3	-		
Turn-on Delay Time ²	$\text{T}_{\text{d(on)}}$	-	17.3	-		
Rise Time	T_r	-	2.8	-	nS	$\text{V}_{\text{DS}}=50\text{V}$ $\text{I}_D=1\text{A}$ $\text{V}_{\text{GS}}=10\text{V}$ $\text{R}_D=3.3\Omega$
Turn-off Delay Time	$\text{T}_{\text{d(off)}}$	-	50	-		
Fall Time	T_f	-	2.8	-		
Input Capacitance	C_{iss}	-	1077	-	pF	$\text{V}_{\text{GS}}=0$ $\text{V}_{\text{DS}}=15\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	46	-		
Reverse Transfer Capacitance	C_{rss}	-	32	-		
Gate Resistance	R_g	-	2	3	Ω	$f = 1.0\text{MHz}$
Source-Drain Diode						
Continuous Source Current ^{1,4}	I_s	-	-	9	A	$\text{V}_G = \text{V}_D = 0$, Force Current
Pulsed Source Current ^{2,4}	I_{SM}	-	-	18	A	
Diode Forward Voltage ²	V_{SD}	-	-	1.2	V	$\text{I}_s=1\text{A}, \text{V}_{\text{GS}}=0$

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. The power dissipation is limited by 150°C junction temperature.
4. The data is theoretically the same as ID and IDM , in real applications, should be limited by total power dissipation

DEVICE CHARACTERISTICS

YS09N10D

CHARACTERISTIC CURVES

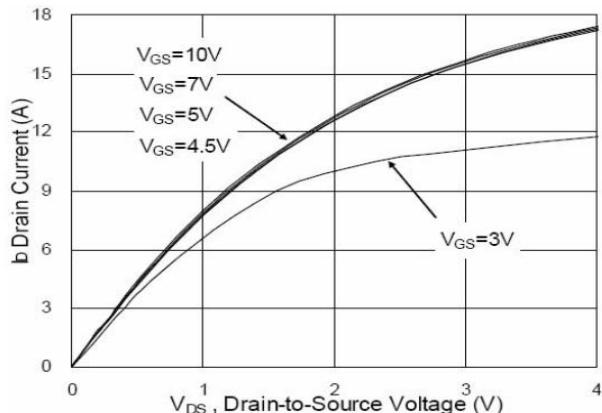


Fig.1 Typical Output Characteristics

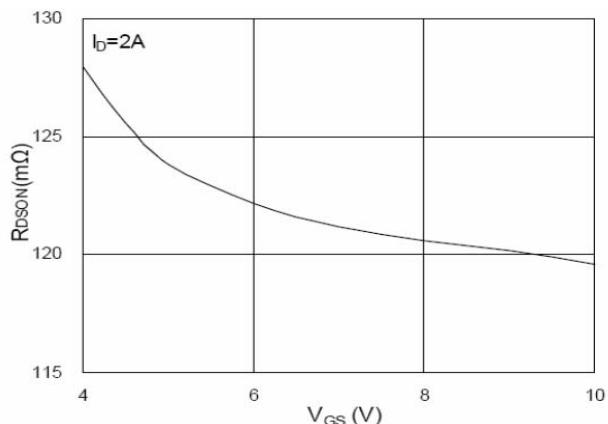


Fig.2 On-Resistance vs. Gate-Source

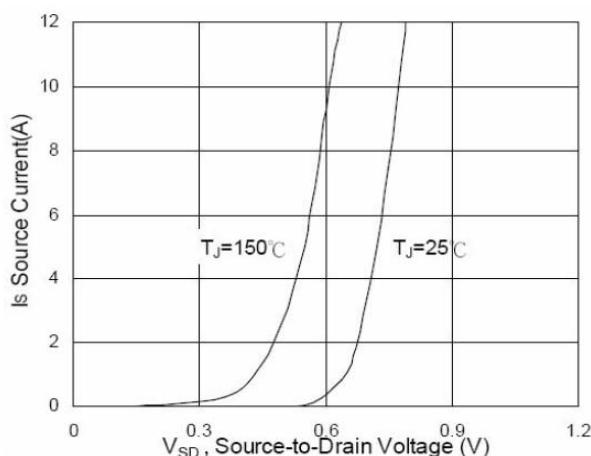


Fig.3 Forward Characteristics Of Reverse

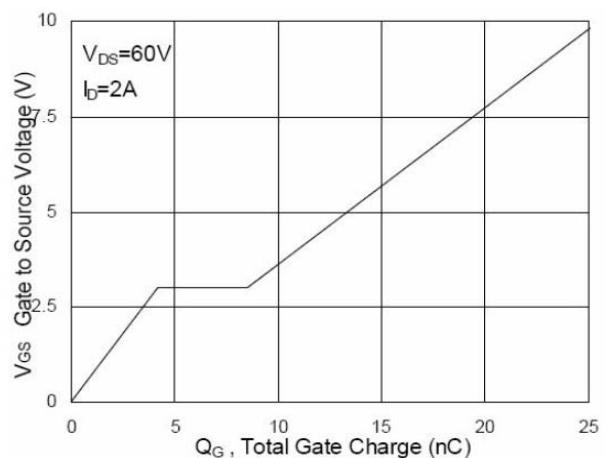


Fig.4 Gate-Charge Characteristics

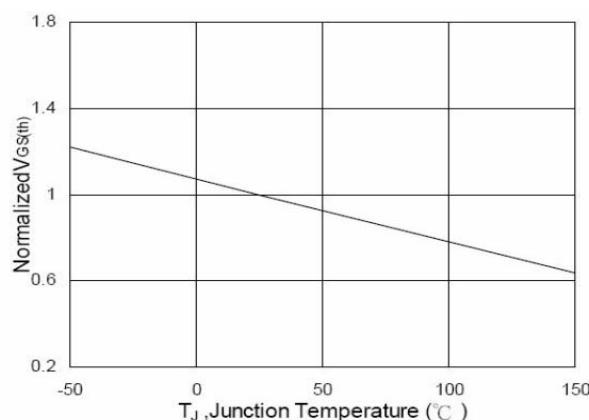


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

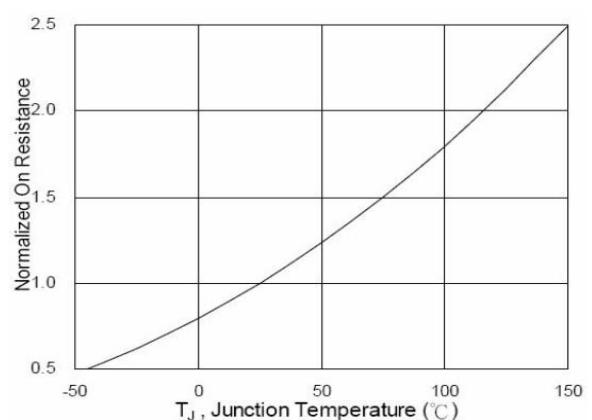


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

DEVICE CHARACTERISTICS

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CHARACTERISTIC CURVES

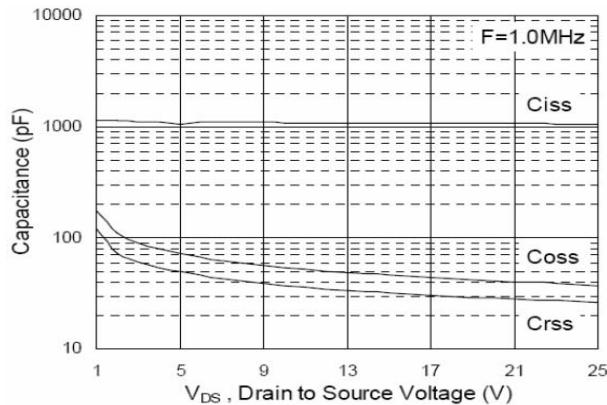


Fig.7 Capacitance

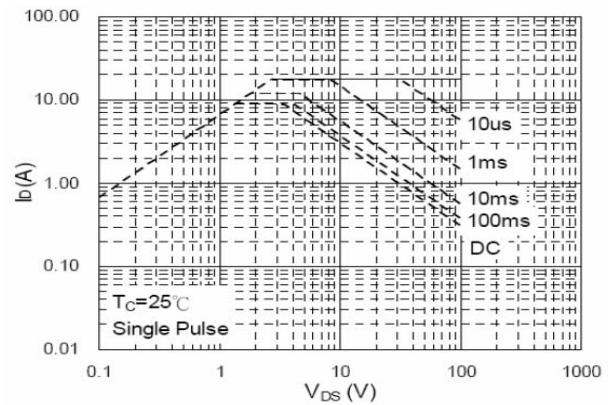


Fig.8 Safe Operating Area

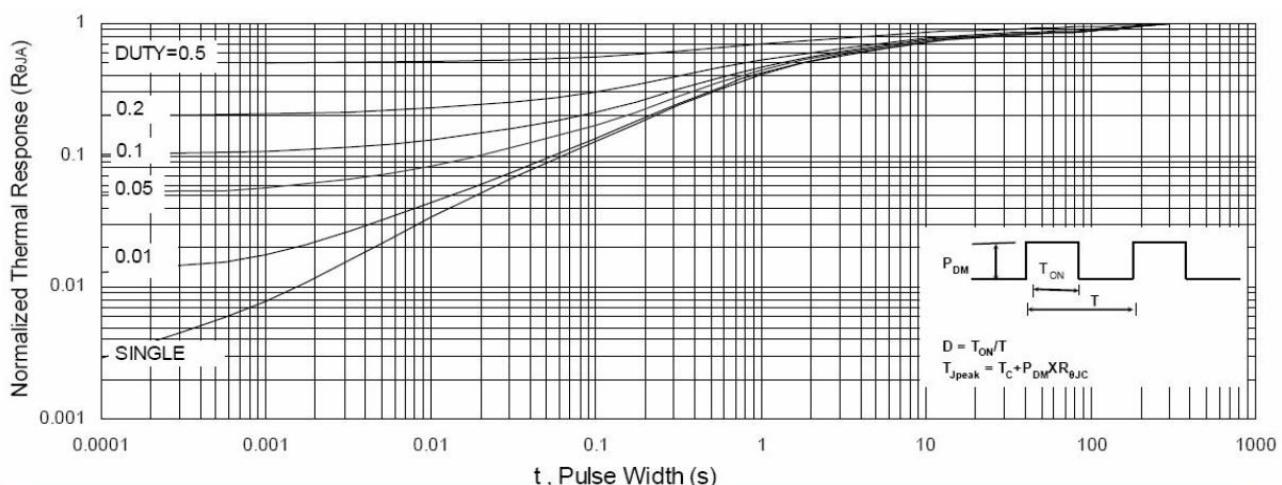


Fig.9 Normalized Maximum Transient Thermal Impedance

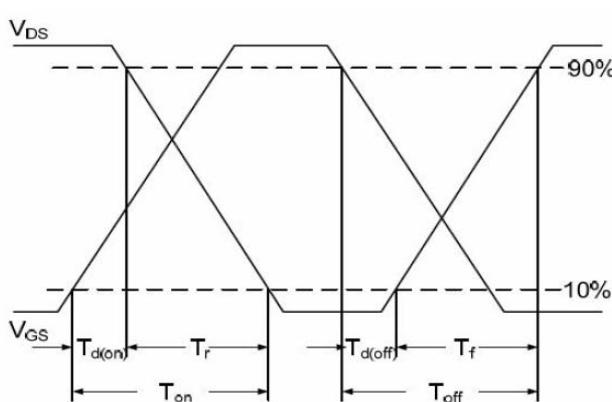


Fig.10 Switching Time Waveform

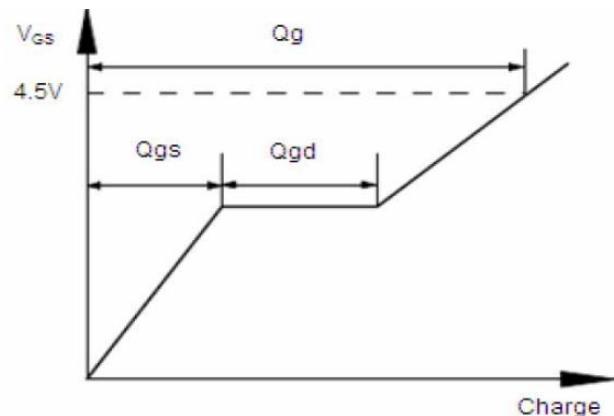


Fig.11 Gate Charge Waveform