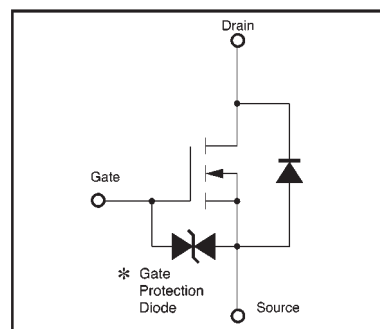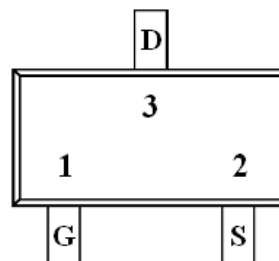![YS SEMICONDUCTOR logo]

DATA SHEET

2N7002E-A

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Pb H

FEATURES

- Low On-Resistance
- Fast Switching Speed
- Low-voltage drive
- Easily designed drive circuits
- Can protect against static electricity 1KV when the product is in use.
- AEC-Q101 qualified

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∗ A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use.
Use the protection circuit when fixed voltages are exceeded.

Maximum Ratings @ T_A=25℃ unless otherwise specified

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage	Continuous	V_{GSS}	±20	V
Drain Current	Continuous	I_D	115	mA
	Pulsed	I_{DP} *1	800	mA
Reverse drain current	Continuous	I_{DR}	115	mA
	Pulsed	I_{DRP} *1	800	mA
Total Power Dissipation		P_d *2	225	mW
Channel temperature		Tch	150	℃
Storage Temperature Range		Tstg	-55 to +150	℃

* 1 PW 10uS, Duty cycle 1%
* 2 When mounted on a 1*0.75*0.062 inch glass epoxy board.

DEVICE CHARACTERISTICS

2N7002E-A

Electrical Characteristics @ T_A=25℃ unless otherwise specified, per element

Characteristic	Symbol	Min	Typ	MAX	Unit	Test Condition
OFF CHARACTERISTICS(Note 2)						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	60			V	V_{GS}=0V, I_D=10μA
Zero Gate Voltage Drain Current	I_{DSS}			1.0	μA	V_{DS}=60V, V_{GS}=0V
Gate-source Leakage	I_{GSS}			±10	μA	V_{GS}=±20V, V_{DS}=0V
ON CHARACTERISTICS(Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.85	2.5	V	V_{DS}=10V, I_D=1mA
Static Drain-Source On-Resistance	$R_{DS(ON)}$			7.5	Ω	V_{GS}=10V, I_D =0.5A
				7.5		V_{GS}=10V, I_D=0.05A
Forward transfer admittance	g_{fs} *	80			mS	V_{DS}=10V, I_D=0.2A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iSS}		25	50	pF	V_{DS}=25V
Output Capacitance	C_{OSS}		10	25	pF	V_{GS}=0V
Reverse Transfer Capacitance	C_{rSS}		3.0	5.0	pF	f=1.0MHz
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$T_{D(ON)}$ *		12	20	nS	I_D=0.2A,V_{DD}=30V,
Turn-Off Delay Time	$T_{D(OFF)}$*		20	30	nS	V_{GS}=10v,RL=150Ω,RG=10Ω

* Pw ≦ 300 μs, Duty cycle ≦ 1%

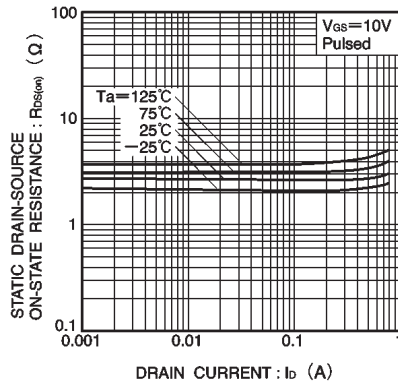# DEVICE CHARACTERISTICS

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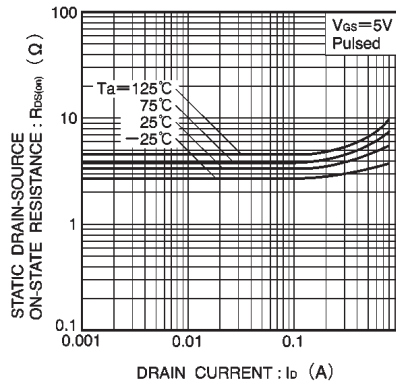Fig.4 Static drain-source on-state resistance vs. drain current (I)

Fig.5 Static drain-source on-state resistance vs. drain current (II)
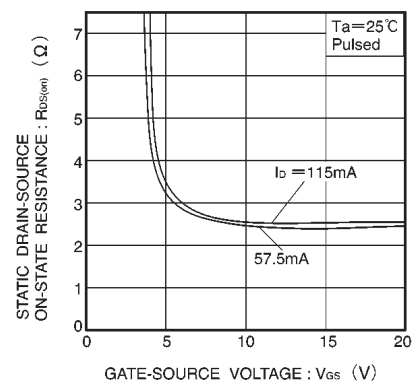

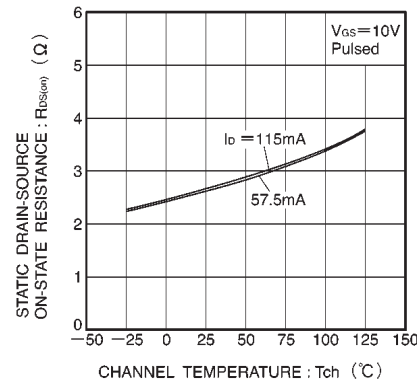Fig.6 Static drain-source on-state resistance vs. gate-source voltage

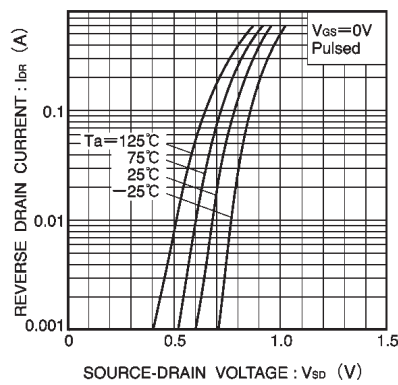Fig.7 Static drain-source on-state resistance vs. channel temperature

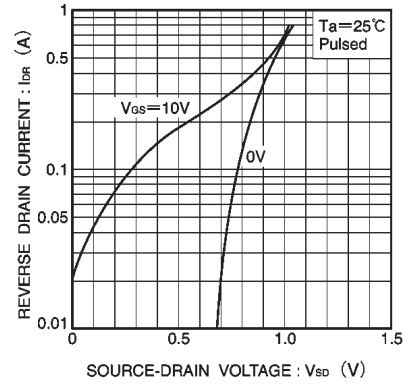Fig.8 Reverse drain current vs. source-drain voltage (I)

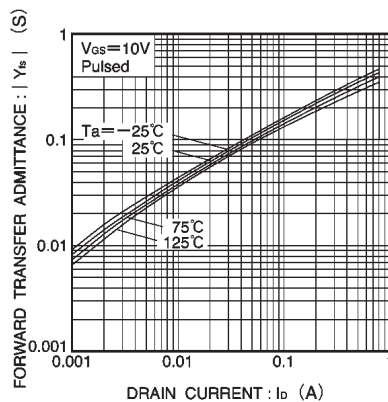Fig.9 Reverse drain current vs. source-drain voltage (II)

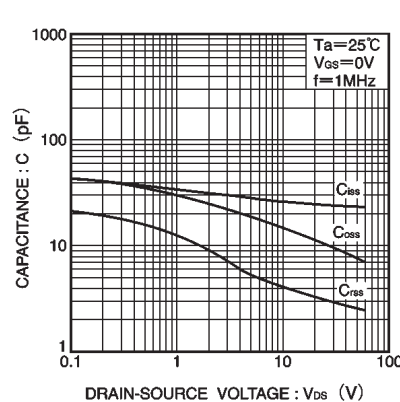Fig.10 Forward transfer admittance vs. drain current

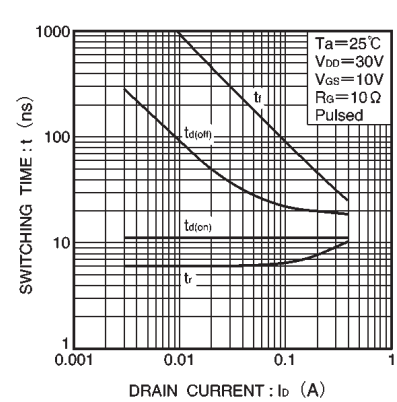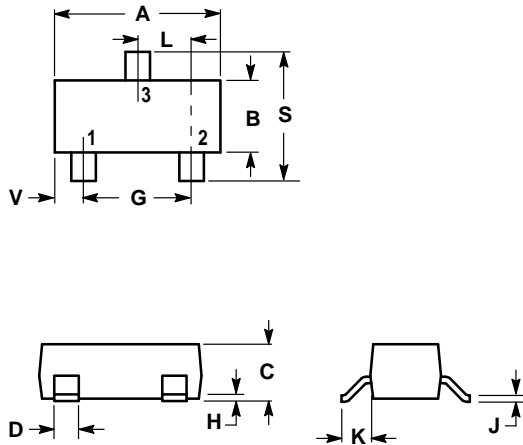Fig.11 Typical capacitance vs. drain-source voltage

Fig.12 Switching characteristics (See Figures 13 and 14 for the measurement circuit and resultant waveforms)
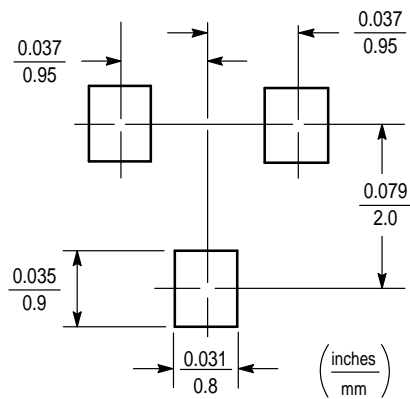
PACKAGE OUTLINE & DIMENSIONS

2N7002E-A

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NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI
   Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

$\frac{0.037}{0.95}$

$\frac{0.037}{0.95}$

$\frac{0.079}{2.0}$

$\frac{0.035}{0.9}$

$\frac{0.031}{0.8}$

$\left(\frac{\text{inches}}{\text{mm}}\right)$

Marking Information

RS = Device code

M = Date code

RS M